Abstract

The present invention generally relates to a NAND-type magnetoresistive RAM, and more specifically, to a NAND-type magnetoresistive RAM comprising a plurality of transistors connected in series as a NAND-type which can reduce the effective area per cell. Two or more NAND-type transistors sharing an adjacent source region and an adjacent drain region are connected in series, thereby reducing inactive regions. A read node connected to a bitline is shared by a plurality of transistors, thereby improving a read operation. As a result, the effective area per cell can be decreased, and the integration of a device can be improved.